What is claimed is:

1. A PDP comprising:

a pair of sustain electrodes formed at a peripheral portion of an upper substrate; and

a trigger electrode formed at the center of the upper substrate.

2. A method for driving a PDP including a reset period, an address period, and a sustain period, comprising the steps of:

supplying a reset pulse to a trigger electrode formed at the center of an upper substrate during the reset period;

supplying a scan pulse to the trigger electrode during the address period;

supplying a data pulse synchronized with the scan pulse to an address electrode formed on a lower substrate opposing the upper substrate during the address period;

alternately applying a sustain pulse to a pair of sustain electrodes formed at a peripheral portion of the upper substrate during the sustain period; and

applying a trigger pulse to the trigger electrode during the sustain period.

3. The method of claim 2, further comprising the step of supplying a direct current voltage to the address electrode during the reset period.

4. The method of claim 2, wherein the trigger pulse has a frequency higher n times than that of the sustain pulse.

5. The method of claim 2, wherein the trigger pulse has a frequency higher two times than that of the sustain pulse.

6. The method of claim 2, wherein the trigger pulse is synchronized with the sustain pulse applied to the pair of the sustain electrodes and then is supplied to the trigger electrode.

7. The method of claim 2, wherein the trigger pulse has a lower voltage level than the sustain pulse.

8. The method of claim 2, further comprising the step of supplying the scan pulse to one of the pair of the sustain electrodes during the address period.